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Title:

BURIED DIGIT SPACER-SEPARATED CAPACITOR ARRAY

Inventor:

Darwin A. Clampitt

Dickstein Shapiro Morin
& Oshinsky LLP
2101 L Street NW
Washington, DC 20037-
1526
(202) 785-9700

BURIED DIGIT SPACER SEPARATED CAPACITOR ARRAY

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor integrated circuits and, in particular, to capacitor arrays formed over the bit line of an integrated circuit substrate.

BACKGROUND OF THE INVENTION

The current semiconductor industry has an ever-increasing pressure for achieving higher device density within a given die area. This is particularly true in memory circuit fabrication, for example Dynamic Random Access Memory (DRAM) manufacturing. A memory cell of a typical DRAM includes a storage capacitor and a charge transfer field effect transistor. The binary data is stored as electrical charge on the storage capacitor in the individual memory cell.

In the early days of DRAM development, planar-type storage capacitors were used which occupied large substrate areas. These were later replaced with container capacitors which occupied less surface area. Recently, however, with the number of memory cells on the DRAM chip dramatically increasing, the miniaturization of DRAM devices requires smaller capacitor features as well as increased storage capacitance.

Different approaches have been employed to achieve higher storage capacitance on a given die area to meet the demands of increasing packing density. For example, with trench capacitors, electrical charge has been stored in capacitors formed vertically in a trench that requires a deep trench formation, but this encounters significant processing difficulties. Another approach is to build a stacked container storage capacitor over at least a portion of the transistor to allow, therefore, smaller cells to be built without losing storage capacity. Stacked capacitors have become increasingly accepted in the semiconductor art. However, as the device density continues to increase, the planar surface area required for building the conventional stacked capacitors must be further reduced. Further, the topography of currently fabricated devices requires more difficult planarization processes to be performed on the DRAM devices.

Accordingly, there is a need for an improved method for fabricating stacked capacitors that minimizes the drawbacks of the prior art. There is also a need for stacked capacitors which have minimal spacing that is not afforded by current photolithographic feature sizes.

SUMMARY OF THE INVENTION

The present invention provides a method for forming stacked capacitors in high density, in which a plurality of patterned capacitor outlines in the form of walls, are formed over the bit line of a semiconductor device. In one aspect of the invention, spacers are formed

on the patterned capacitor walls and become part of the cell polysilicon after being covered with cell nitride. In another aspect, the spacers are formed of a material capable of being etched back, such as titanium nitride. In another aspect, a metal layer is patterned and annealed to a polysilicon layer to form a mask for a capacitor array, and subsequently etched to form the array.

Additional features and advantages of the present invention will be more clearly apparent from the detailed description which is provided in connection with accompanying drawings which illustrate exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic sectional view of a semiconductor wafer fragment illustrating a base structure for forming the first embodiment of the invention.

FIG. 2 is a side sectional view of the FIG 1 semiconductor wafer fragment after initial processing steps for forming the first embodiment of the invention.

FIG. 3 is a side sectional view of the FIG.2 structure at a subsequent stage of fabrication.

FIG. 4 is a top view of FIG. 3.

FIG. 5 is a side sectional view of the FIG. 3 structure at a subsequent stage of fabrication.

FIG. 6 is a top view of FIG. 5.

FIG. 7 is side sectional view of the FIG. 5 structure at a subsequent stage of fabrication.

FIG. 8 is a side sectional view of the FIG. 7 structure at a subsequent stage of fabrication.

FIG. 9 is a top view of FIG. 8.

FIG. 10 is a side sectional view of the FIG. 8 structure at a subsequent stage of fabrication.

FIG. 11 is a side sectional view of the FIG. 10 structure at a subsequent stage of fabrication.

FIG. 12 is a side sectional view of the FIG. 11 structure at a subsequent stage of fabrication.

FIG. 13 is a side sectional view of the FIG. 12 structure at a subsequent stage of fabrication.

FIG. 14 is a side sectional view of the FIG. 13 structure at a subsequent stage of fabrication.

FIG. 15 is a side sectional view of the FIG. 11 structure at a subsequent stage of fabrication.

FIG. 16 is a side sectional view of the FIG. 15 structure at a subsequent stage of fabrication.

FIG. 17 is a side sectional view of the FIG. 16 structure at a subsequent stage of fabrication.

FIG. 18 is a side sectional view of the FIG. 17 structure at a subsequent stage of fabrication.

FIG. 19 is a side sectional view of the FIG. 14 structure at a subsequent stage of fabrication.

FIG. 20 is a diagrammatic sectional view of a semiconductor wafer fragment illustrating a base structure for forming another embodiment of the invention.

FIG. 21 is a side sectional view of the FIG. 20 structure at a subsequent stage of fabrication.

FIG. 22 is a side sectional view of the FIG. 21 structure at a subsequent stage of fabrication.

FIG. 23 is a side sectional view of the FIG. 22 structure at a subsequent stage of fabrication.

FIG. 24 is a side sectional view of the FIG. 23 structure at a subsequent stage of fabrication.

FIG. 25 is a side sectional view of the FIG. 20 structure at a subsequent stage of fabrication.

FIG. 26 is a diagrammatic sectional view of a semiconductor wafer fragment illustrating a base structure for forming another embodiment of the invention.

FIG. 27 is a side sectional view of the FIG. 26 structure at a subsequent stage of fabrication.

FIG. 28 is top view of FIG. 27.

FIG. 29 is a side sectional view of the FIG. 27 structure at a subsequent stage of fabrication.

FIG. 30 is top view of the FIG. 29 structure at a subsequent stage of fabrication.

FIG. 31 is a side sectional view of the FIG. 29 structure at a subsequent stage of fabrication.

FIG. 32 is a perspective view of the FIG. 31 structure.

FIG. 33 is a side sectional view of the FIG. 31 structure at a subsequent stage of fabrication.

FIG. 34 is a side sectional view of the FIG. 33 structure at a subsequent stage of fabrication.

FIG. 35 is a side sectional view of the FIG. 34 structure at a subsequent stage of fabrication.

FIG. 36 is a top view of the FIG. 35 structure.

FIG. 37 is a side sectional view of the FIG. 35 structure at a subsequent stage of fabrication.

FIG. 38 is a side sectional view of the FIG. 37 structure at a subsequent stage of fabrication.

FIG. 39 is a side sectional view of the FIG. 38 structure at a subsequent stage of fabrication.

FIG. 40 is a side sectional view of the FIG. 39 structure at a subsequent stage of fabrication.

FIG. 41 is a perspective view of the FIG. 40 structure.

FIG. 42 is a diagram of a computer system according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural and electrical changes may be made without departing from the spirit or scope of the present invention.

The term "substrate" used in the following description may include any semiconductor-based structure that has a semiconductor surface. The term should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), silicon-on-nothing (SON), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to a "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in or on the base semiconductor or foundation.

Referring now to the drawings, where like elements are designated by like reference numerals, Figure 1 depicts a portion of a memory cell

construction for a DRAM at an intermediate stage of the fabrication, in which stacked capacitors are to be formed in accordance with the present invention. A pair of memory cell access transistors 33 are formed within and over a doped well 13 of a substrate 12. The well may be a p-well or n-well depending on the type of transistor 33. The well 13 and the pair of transistors 33 are surrounded by a trench isolation region 14 that provides isolation. N-type active regions 16 are provided in the doped p-type well 13 of substrate 12 (for NMOS transistors) and the pair of access transistors have respective gate stacks 30. The gate stacks 30 include an oxide layer 18, a conductive layer 20, such as a doped polysilicon layer with tungsten silicide on it, nitride sidewall spacers 32, and a nitride cap 22. Additional stacks 31 may also be formed for use in performing self aligned contact etches to form conductive plugs 50, 50a for capacitor structures in the region between stacks 30, 31. The details of these steps are well-known in the art and are not described in detail herein.

Polysilicon plugs 50, 50a (Figure 1) are formed in a contact opening of a first insulating layer 24, to directly connect to a source or drain region 16 of the semiconductor device. The first insulating layer 24 could be, for example, borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Once the polysilicon plugs 50, 50a are formed, the whole structure, including the substrate 12 with the gate stacks 30, the first insulating layer 24 and the polysilicon plugs 50, 50a is CMP polished to provide a planarized surface.

At this point, a second insulating layer 25, which can be of the same material as that of the first insulating layer 24, is deposited over the first insulating layer 24 and the polysilicon plugs 50, 50a. A contact opening or

via is etched over the polysilicon plug 50a and a conductive layer or inter-connection layer 55 is then deposited and patterned to connect to polysilicon plug 50a, as illustrated in Figure 1. The inter-connection layer 55 functions as a digit line. The digit line is made of, for example, a polysilicon, titanium nitride, or a tungsten material with a nitride cap.

Referring now to figure 2, a third insulative layer 60 is formed over the inter-connection layer 55. The third insulative layer 60 could be, for example, BPSG, BSG, or PSG. The polysilicon plugs 50, that are not in contact with the digit line 55, are made to extend through the third insulative layer 60. The contact holes for the polysilicon plugs in layer 60 are made using conventional photolithographic techniques and plasma etching. For example, the etching can be carried out in a reactive ion etcher (RIE) using an etchant gas mixture containing fluorine, such as C_5F_8, C_4F_8, CHF_3, CO, O_2, and Ar.

A layer of conductively doped polysilicon is deposited over layer 60 to fill the contact holes and provide conductive plugs 61, and subsequently etched back to expose layer 60. The conductive plugs 61 are electrically isolated from the digit line 55, for example, by nitride spacers (not shown). The details of these steps are well-known in the art and other methods may be used.

Next, an etch stop layer 64 is deposited over the third insulative layer 60. The etch stop layer 64 could be, for example, a nitride, or another dielectric etch stop layer. A thick layer 68 of BPSG, or other insulative material, is then deposited over the etch stop layer 64. The layer 68 of BPSG is etchably different from the etch stop layer 64. On top of

layer 68, a layer 70 of polysilicon is deposited. Layers 68 and 70 are also substantially etchably different.

One patterning option for forming capacitors of the present invention is to create alternating polysilicon rectangles in the polysilicon layer 70. This can be accomplished, for example, by patterning with resist and etching the polysilicon layer 70 to form a square or rectangular checker board pattern. This etching step etches through the polysilicon layer 70 but stops at the BPSG layer 68. The result of this etching step is a checker board pattern of square polysilicon blocks 70c, as illustrated in Figures 3 and 4. Alternatively, the patterning can be used to create an alternating pattern of rectangular shaped blocks, or oval shaped blocks, illustrated by dashed lines 70d and 70e, respectively, in Figure 4.

Next, sidewall spacers 80 are formed on the sidewalls of alternating square, rectangular, or oval blocks 70c, 70d and 70e, as shown in Figures 5 and 6. The spacers 80 are formed by depositing a polysilicon layer over the polysilicon blocks 70c, 70d, or 70e (hereinafter collectively referred to as "blocks 70c"), and subsequently anisotropically etching to provide a plurality of sidewall spacers 80 on all vertical surfaces of alternating blocks 70c. Collectively, the sidewall spacers 80 and polysilicon blocks 70c define an array of structure profiles which will be transferred into at least one of the underlying layers.

In another patterning option, the square, rectangular, or oval checker board pattern of Figures 5 and 6 can be printed with photoresist onto the BPSG layer 68. Blocks 70c and spacers 80 would be comprised of photoresist. With this option, the minimum corner to corner spacing

between the photoresist square or rectangular blocks would have to be maintained without bridging.

Next, with reference to Figure 7, the BPSG layer 68 is selectively and anisotropically etched down to the nitride etch stop layer 64 to form BPSG blocks 68a. Care should be taken during this step to overetch enough to clear the BPSG material out from between the corners of the blocks to prevent possible cell node to cell node shorts. The polysilicon spacers 80 and remaining polysilicon blocks 70c (or 80 and 70c comprised of photoresist) are then selectively removed by suitable methods such as chemical-mechanical polish (CMP), or wet or dry etching, which are well known in the art.

Referring now to Figures 8 and 9, a spacer 90 is deposited on the vertical walls of the BPSG blocks 68a. The spacer 90 must be wide enough to bridge together at the corners of BPSG blocks 68 to isolate individual squares, rectangles, or ovals in order to prevent the possibility of cell node to cell node shorts. The width W of spacer 90 should be greater than distance D of Figure 6. The spacer 90 material is preferably either titanium nitride, polysilicon, or another material etchably different from the BPSG blocks 68a. The spacer 90 material may also comprise platinum. Alternatively, the material for blocks 68a (material layer 68) can comprise any material that is etchably different from the spacer material 90. The material 68 can be chosen to be a material that may remain on the periphery of the integrated circuit without the need to remove it during subsequent process steps.

The BPSG blocks 68a are then selectively etched away down to the nitride etch stop layer 64, shown in Figure 10, preferably using a wet etch

leaving the spacers 90 intact. The periphery is covered with resist during this step to prevent removal of BPSG from other areas. At this point the spacers 90 are in the form of a square, rectangular, or oval honeycomb pattern. Thereafter, as shown in Figure 11, the etch stop layer 64 is selectively etched or otherwise removed using spacers 90 as a pattern utilizing techniques well known in the art.

If the spacer material used for spacers 90 is titanium nitride and it is desirable to increase its thickness, another layer of titanium nitride 90a is deposited over existing spacers 90 and spacer etched, as seen in Figure 12. Alternatively, titanium nitride can be deposited in one step in a layer of sufficient thickness approximately equal to layer 90 and the two layers 90a. During this etching process the portions of newly deposited titanium nitride spacer 90a covering the insulative layer 60 are overetched so as to expose a direct electrical contact with polysilicon plugs 61.

Next, with reference to Figure 13, a hemispherical grain (HSG) polysilicon 92 is deposited over the spacers 90 and 90a, and exposed polysilicon plugs 61. This rough polysilicon layer 92 forms the cell node of a capacitor. The rough HSG layer 92 increases the surface area of the storage node which improves the cell's capacitance. The upper portion of the HSG layer 92 is then removed by chemical-mechanical polish (CMP) or dry etching, as well known in the art, to isolate the top portion of the titanium nitride layers, designated by reference numeral 94. The titanium nitride 90, 90a is then selectively removed by etching with a piranha (sulfuric/hydrogen peroxide) process, or other selective etch process, to isolate the containers 93 formed by the remaining HSG layer, as shown in Figure 14. Then, as well known in the art, a cell nitride dielectric and a

capacitor upper electrode may be deposited to form capacitors in the containers 93. For example, as noted, Hemispherical Grain (HSG) Polysilicon 92 can be deposited to form the bottom cell plate of the capacitor, followed by deposition of a dielectric layer such as a nitride, followed by deposition of an upper electrode.

Referring back to Figure 8, if the spacer material used for spacers 90 is polysilicon, then a thin layer of silicon nitride 90b is deposited over the polysilicon spacers 90, as shown in Figure 15. Then, referring to Figure 16, a layer of polysilicon 90c is deposited over the silicone nitride layer 90b. The polysilicon layer 90c is anisotropically etched along with the layer of silicon nitride 90b, etch stop layer 64, and an upper portion of insulating layer 60 to define containers 91, as shown in Figure 17. During this etching process the portions of newly deposited polysilicon layer 90c covering the etch stop layer 64 are overetched so as to expose a direct electrical contact with polysilicon plugs 61.

Hemispherical grain (HSG) polysilicon 92 is then deposited over the spacers 90, 90b, and 90c, and exposed polysilicon plugs 61. The containers 91 are then filled with photoresist and the HSG layer 92 is removed by chemical-mechanical polish (CMP) or dry etching to expose the horizontal surfaces of layers 90, 90b, and 90c, as shown in Figure 18. Then, as well known in the art, cell nitride and an upper capacitor electrode may be deposited to form capacitors in the containers 91, as discussed above. During subsequent processing steps, electrical connections may established between an upper capacitor electrode and polysilicon spacer 90, to enable the spacer to become part of the cell plate of the capacitor.

Another way to form capacitors, utilizing the disclosed patterning techniques, is by utilizing the above disclosed structures of Figures 14 and 18 with barriers, metal electrodes, and cell plates with dielectrics having high dielectric constants. For example, with reference to Figure 19, a metal insulator silicon (MIS) capacitor can be formed as follows. An ammonia anneal is performed on the wafer to nitridize the surface of the HSG polysilicon 92. Thereafter, if the sidewall spacers 90 (Figures 10-14) are titanium nitride spacers, a cell dielectric layer 95, such as tantalum pentoxide (Ta_2O_5), is deposited over the polysilicon surface 92. A cell plate of titanium nitride 97 is deposited over the dielectric layer 95. A layer of polysilicon 99 is then deposited over layer 97 to prevent oxidation of the titanium nitride layer 97 during subsequent steps such as deposition of BPSG. In the above example, if the sidewall spacers 90 are polysilicon spacers (Figures 10, 15-18), then Ta_2O_5 is substituted for silicon nitride in layer 90b of Figure 18.

Another way of forming capacitors in the present invention is by forming metal insulator metal (MIM) capacitor structures. With reference to Figure 20, after conductively doped polysilicon is deposited over layer 60 to fill the contact holes and provide conductive plugs 61, the polysilicon is overetched so that the plugs 61 are recessed below the surface of the layer 60. A layer of conductive barrier material 101, such as tantalum nitride or tantalum silicon nitride, is deposited over the layer 60 and subsequently removed by etching or CMP to expose the layer 60 and the conductive barrier layer 101 on top of the plugs 61. Thereafter, layers 64, 68, and 70 are deposited and patterned as discussed above.

If the sidewall spacers 90 are titanium nitride spacers, the conductive barrier layer 101 is exposed during the etching steps described above, as shown in Figure 21. Thereafter, with reference to Figures 22 and 23, a layer of platinum 103 is deposited over the titanium nitride sidewall spacers 90 (or 90 and 90a). Platinum cell nodes are then electrically isolated by filling with resist, and the top surfaces of spacers 90 (or 90 and 90a) are exposed by dry etching, or CMP, to remove the portion of the platinum layer 103 covering the spacers. Then, the spacers 90 (or 90 and 90a) are removed as described above. The resist covering the platinum cell nodes is also subsequently removed. The MIM capacitor is formed, with reference to Figure 24, by depositing a dielectric layer 105 having a high dielectric constant, such as Ta_2O_5 or BST, over layer 103. Then a platinum cell plate 107 is deposited over dielectric layer 105. The platinum material in layers 103 and 107 may be substituted with other suitable materials, for example, ruthinium oxide, rhodium, or platinum rhodium.

Where the sidewall spacers 90 are not titanium nitride spacers, such as polysilicon sidewall spacers described above, the MIM capacitors are formed as follows. With reference to Figures 15, 16, and 17, a sidewall spacer made of platinum is deposited as sidewall spacer 90, instead of a polysilicon spacer. Then, a Ta_2O_5 or barium strontium titanate (BST) dielectric, or another high dielectric constant dielectric, is deposited as layer 90b. A platinum layer is deposited as layer 90c. The MIM capacitor structure is then completed as follows. With reference to Figure 25, a platinum cell node layer 107 is deposited, and the cell nodes are filled with resist. Thereafter, the platinum cell node layer 107 is etched back to

electrically isolate each cell capacitor, exposing the tops of spacers 90, 90b, and 90c, and the resist is removed from the cell nodes.

The cell node layer 107 is electrically isolated from spacers 90 and neighboring cell nodes, as shown in Figure 25. A Ta_2O_5 cell dielectric layer 108 is then deposited over cell nodes 107 and exposed spacers 90, 90b, and 90c. A platinum cell plate 109 is deposited over the dielectric layer 108.

In subsequent processing steps, cell plate 109 can be electrically connected to the spacer(s) 90. This can be accomplished, for example, by forming contact holes through layers 108 and 109 to the spacer(s) 90 using a reactive ion etching process, as described above. The contact holes could then be filled with a conductive material to electrically connect the spacer(s) 90 to the cell plate 109. The aforementioned connections can be made at the edges of memory arrays, thereby making spacer(s) 90 part of the cell plate of the capacitor.

In another embodiment of the present invention, the square or rectangular block honeycomb sidewall pattern can be achieved by silicide patterning. With reference to Figure 26, a structure is formed according to methods well known in the art, and as discussed above, having a digit line 55, and cell node plugs 61, having contacts rising above the digit line 55, in a layer 60, which may be BPSG. A conductive barrier layer 101, as shown Figure 20, may be formed if so required by the resulting capacitor structure. A layer 164 consisting of nitride is deposited over layer 60. A thick layer 168 of phosphosilicate glass (PSG) or BPSG is deposited over layer 164. On top of layer 168 is deposited a layer 170 of polysilicon, and a layer 174 of TEOS.

A layer of patterned photoresist 72 is formed over the TEOS layer 174, as shown in Figures 27 and 28, to define a first series of trenches 74. With reference to Figure 29, the patterned photoresist 72 is used to etch trenches 175 in the TEOS layer 174. The trenches 175 are etched over every other row of the cell node polysilicon plugs 61, and the etching is down to and stops at the polysilicon layer 170. The photoresist 72 is subsequently removed. As shown in Figure 30, another layer of patterned photoresist 76 is deposited to define a second series of trenches 77 that are perpendicular to the trenches 175 etched into the TEOS layer 174. Reference numeral 70a represents rows of the TEOS layer, beneath the photoresist 76, that have not been etched (covered by photoresist 72 in the prior etching step). The second series of photoresist rows run over every other line of cell node polysilicon plugs 61. The second series of photoresist trenches are used to etch trenches in polysilicon layer 170 in a two step etch. The first step etch is a selective anisotropic etch through the exposed polysilicon layer 170. Then, a selective oxide etch is performed to remove the TEOS layer 174 from the polysilicon layer 170. This etch is performed down into the BPSG or PSG layer 168. Therefore, subsequent to etching the second row of trenches, remaining portions of the TEOS layer 174 are removed from the top the polysilicon layer 170 by an oxide etch or another suitable method, as seen in Figure 31.

The effect of etching the two transverse series of trenches is illustrated in Figure 32, and forms a block checker board pattern. The resulting structure is comprised of an array of trenches, or an alternating square, rectangular, or oval checker pattern having higher elevations of TEOS layer areas 70c, and intermediate elevations of polysilicon 70b.

Figure 32 also shows the underlying layer of BPSG 168. The alternating square or rectangular checker pattern is comprised of three different elevations due to the two separate etching steps: some portions have been etched twice (down to the BPSG layer 168), some portions once, forming areas 70b, and other portions not etched at all, forming areas 70c. Alternatively, the aforementioned techniques can be used to form alternating oval structures (not shown). The above steps used to form the alternating block pattern are discussed in detail in U.S. Patent No. 6,087,263, the disclosure of which is incorporated herein by reference.

Referring now to Figure 33, a metal layer 178 is deposited over the top surface of the block pattern. The metal deposited should be one that easily forms a silicide. An exemplary material for metal layer 178 would be titanium, paladium, or tungsten. A silicide is then formed by annealing the metal layer 178 with the polysilicon layer 170 where the two layers are in direct contact.

Next, with reference to Figure 34, a wet etch is used to remove the portions of the metal layer 178 that did not react with the polysilicon layer 170 to form a metal silicide during the annealing step. The remaining metal portion is the silicide metal layer 180. Any remaining TEOS and polysilicon are subsequently etched away, using any appropriate etching process, thereby leaving behind a silicide block pattern (checker board pattern). The silicide blocks 180 are then isotropically etched back so that the silicide blocks do not bridge together at the corners, as illustrated in Figures 35 and 36.

Using the silicide 180 checkerboard block pattern, as illustrated in Figure 36, as a mask, the BPSG or PSG layer 168 is then selectively and

anisotropically etched down to layer 164 consisting of nitride, or another suitable dielectric etch stop layer, as shown in Figure 37. Thereafter, the silicide blocks 180 are removed either by an etching step or by a chemical-mechanical polish (CMP), leaving BPSG square or rectangular blocks 168 over layer 164.

Next, with reference to Figure 38, a spacer material 182 is deposited over the blocks 168. The spacer material 182 could be TEOS, amorphous silicon, polysilicon, titanium nitride, or another material. The spacer material 182 will be chosen by the artisan depending upon the type of capacitor that will be eventually made in the capacitor containers defined by the spacer material 182. When choosing spacer material 182, consideration must be given to ensure that the spacer material 182 is etchably different from the block material 168, thereby enabling subsequent removal of the block material 168 without damaging the spacer material 182. The spacer material is then spacer etched to create sidewall spacers, as illustrated in Figure 39.

The BPSG or PSG blocks 168 are then removed by an etching process, or other suitable process, leaving a grid of interlocked spacers 182, as illustrated in Figures 40 and 41. The spacers 182 are then covered with layers of materials depending upon the material chosen for the spacers, i.e. titanium nitride or polysilicon, as disclosed above. If the spacer 182 is a amorphous silicon spacer, a process of seeding and annealing the spacer can be performed to form a selective HSG layer, prior to the deposition of the cell nitride layer. The HSG layer will provide the benefit of a greater surface area, resulting in greater capacitance.

Thereafter, various types of capacitors can be formed in the containers, defined by the interlocked spacers 182, over the buried digit line 55. For example, Hemispherical Grain (HSG) Polysilicon can be deposited to form the bottom cell plate of the capacitor, followed by a dielectric layer such as a nitride, an then depositing an upper electrode. As disclosed above, MIS or MIM capacitor structures may also be formed.

Figure 42 illustrates a computer system 300 that may incorporate the benefits of the present invention. The system 300 has a memory circuit 321 including a capacitor array 320 constructed in accordance with the present invention. The system 300 includes a central processing unit (CPU) 302 for performing computer functions, such as executing software to perform desired tasks and calculations. One or more input/output devices 304, 306, such as a keypad or a mouse, are coupled to the CPU 302 and allow an operator to manually input data thereto or to display or otherwise output data generated by the CPU 302. One or more peripheral devices such as a floppy disk drive 312 or a CD ROM drive 314 may also be coupled to the CPU 302. The computer system 300 also includes a bus 310 that couples the input/output devices 312, 314 and the memory circuit 321 to the CPU 302.

While exemplary embodiments of the invention have been described and illustrated, it should be apparent that many modifications can be made to the present inventions without departing from its spirit and scope. For example, the above described checker board pattern could be printed on BPSG, PSG, or another layer, utilizing photoresist patterning, or other patterning techniques. Accordingly the invention is not limited by

the foregoing description or drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is: